ABSTRACT OF THE DISCLOSURE

An apparatus comprising an array of memory cells, a refresh circuit, a first monitor cell, a second monitor cell, and a control circuit. The refresh circuit may be configured to refresh the array of memory cells in response to a refresh control signal. The first monitor cell may be configured to have a charge leakage similar to the memory cells. The second monitor cell may be configured to have a discharge leakage similar to the memory cells. The control circuit may be configured to generate the refresh control signal in response to either a voltage level of the first monitor cell rising above a first pre-determined threshold level or a voltage level of the second monitor cell dropping below a second pre-determined threshold level, where the first and second threshold levels are different.